Listing of Claims:

1. (Original) In a method for addressing and sustaining a PDP wherein an addressing voltage is applied to at least one section S1 of the PDP while at least one other section S2 of the PDP is being simultaneously sustained, the improvement wherein visual artifacts between the sections are reduced by means of gamma corrected subfields with sustains timed to balance the center of light between S1 and S2.

2. (Original) In a method for operating a surface discharge AC plasma display having row scan, bulk sustain, and column data electrodes, the improvement which comprises addressing at least one section S_1 of the AC plasma display while another section S_2 is being simultaneously sustained, each section having a predetermined number of bulk sustain electrodes and row scan electrodes, and wherein visual artifacts between the sections are reduced by means of gamma corrected subfields with sustains timed to balance the center of light between S1 and S2.

3. (Original) The invention of Claim 2 wherein section S_2 is subsequently addressed while section S_1 is being sustained.

4. (Original) The invention of Claim 3 wherein there are 6 to 17 subfields.

5. (Original) The invention of Claim 4 wherein each of the sections S_1 and S_2 is sustained with a different number of sustains per subfield.

6. (Original) The invention of Claim 4 wherein at least one subfield of each section S1 and S2 is sustained with the same number of sustains per subfield.

7. (Original) The invention of Claim 2 wherein the resolution of the plasma display is about 480 to about 1200 row scan electrodes.

8. (Original) The invention of Claim 2 wherein there are 6 to 17 subfields for a resolution up to 768 row scan electrodes.

9. (Original) The invention of Claim 2 wherein the method for the reduction of motion and visual artifacts includes the writing of pixels followed by selective erase.

10. (Original) The invention of Claim 1 wherein there is provided a reset voltage before addressing.

11. (Original) The invention of Claim 10 wherein the reset before addressing is a slow ramp reset voltage.

12. (Original) An AC plasma display having row scan, bulk sustain, and column data electrodes, said display being divided into a plurality of sections S_1, S_2, S_n, each section having a predetermined number of bulk sustain electrodes and row scan electrodes, and electronic circuitry for simultaneously addressing and sustaining at least two different sections of the AC plasma display, the improvement wherein visual artifacts between a section being addressed and a section being simultaneously sustained are reduced by means of gamma corrected subfields with sustains timed to balance the center of light between the sections.

13. (Original) The invention of Claim 12 wherein there is provided a reset voltage before addressing.

14. (Original) The invention of Claim 13 wherein the reset before addressing is a slow ramp reset voltage.

15. (Original) In a system for addressing and sustaining PDP, wherein an addressing voltage is applied to at least one section S1 of the display panel while at least one other section S2 of the panel is being simultaneously sustained, the improvement wherein visual artifacts are reduced by means of gamma corrected subfields with sustains timed to balance the center of light between S1 and S2.

16. (Original) In a system having electronic circuitry for operation of an AC plasma display having row scan, bulk sustain, and column data electrodes, said display being divided into a plurality of sections S_1, S_2, S_n, each section having a predetermined number of bulk sustain electrodes and row scan electrodes the improvement which comprises electronic circuitry for simultaneously addressing and sustaining at least two different sections of the AC plasma display and wherein visual artifacts between a section being addressed and a section being simultaneously sustained are reduced by means of gamma corrected subfields with sustains timed to balance the center of light between the sections.

17. (Original) The invention of Claim 16 wherein there is provided a reset voltage before addressing.

18. (Original) The invention of Claim 17 wherein the reset before addressing is a slow ramp reset voltage.

19. (Canceled)

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44. (Canceled)

45. (Original) In an integrated circuit for receiving and processing digital signals to a display, the improvement wherein the processing includes SAS.

46. (Original) The invention of Claim 45 wherein the processing includes the center of light method.

47. (Canceled)

48. (Canceled)

49. (Canceled)

50. (Canceled)